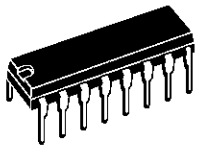
24 STAGE FREQUENCY DIVIDER

- VERY LOW QUIESCENT CURRENT
- HIGH NOISE IMMUNITY
- VOLTAGE SUPPLY RANGE 3V TO 18V
- ALL STAGES ARE RESETTABLE
- RESET DISABLES THE RC OSCILLATOR FOR LOW STANDBY POWER DRAIN
- RC AND CRYSTAL OSCILLATOR OUTPUT ARE CAPABLE OF DRIVING EXTERNAL LOADS

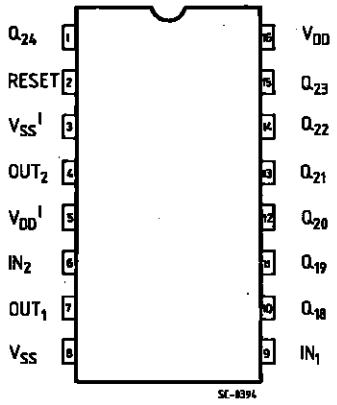


DESCRIPTION

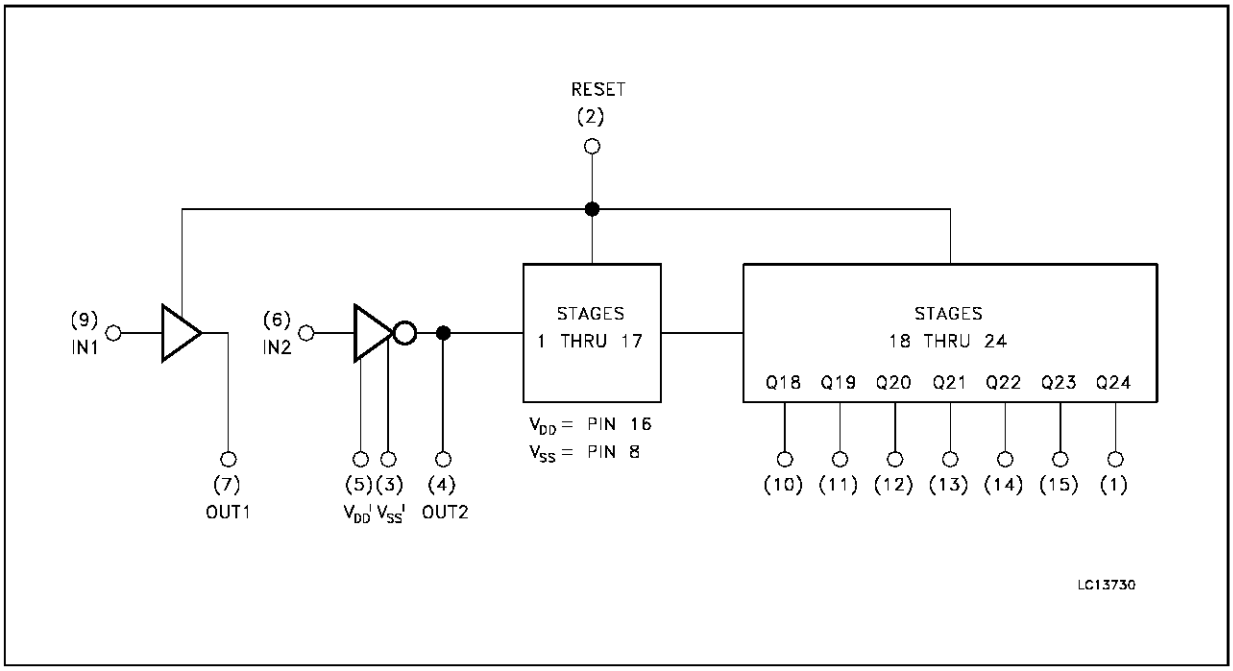
The CC4521 is a monolithic integrated circuit, available in 16-lead dual-in-line plastic package and plastic micro packages.

The CC4521 have a chain of 24 flip-flops with an input circuit that allows three modes of operation. The input circuit functions as a crystal or an RC oscillator or as an input buffer for an external oscillator. Each flip-flop performs a divide-by-two function giving a total count of 2^{24} = 16,777,216. The count advances on the negative going edge of the clock. Access is available to the final seven stages giving the device added flexibility.

PIN CONNECTION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{DD} *	Supply Voltage	-0.5 to +18	V
V_i	Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current (any one input)	± 10	mA
P_{tot}	Total Power Dissipation (per package) Dissipation per Output Transistor for Top = Full Package Temperature Range	200 100	mW mW
T_{op}	Operating Temperature	-40 to +85	°C
T_{stg}	Storage Temperature	-65 to +150	°C

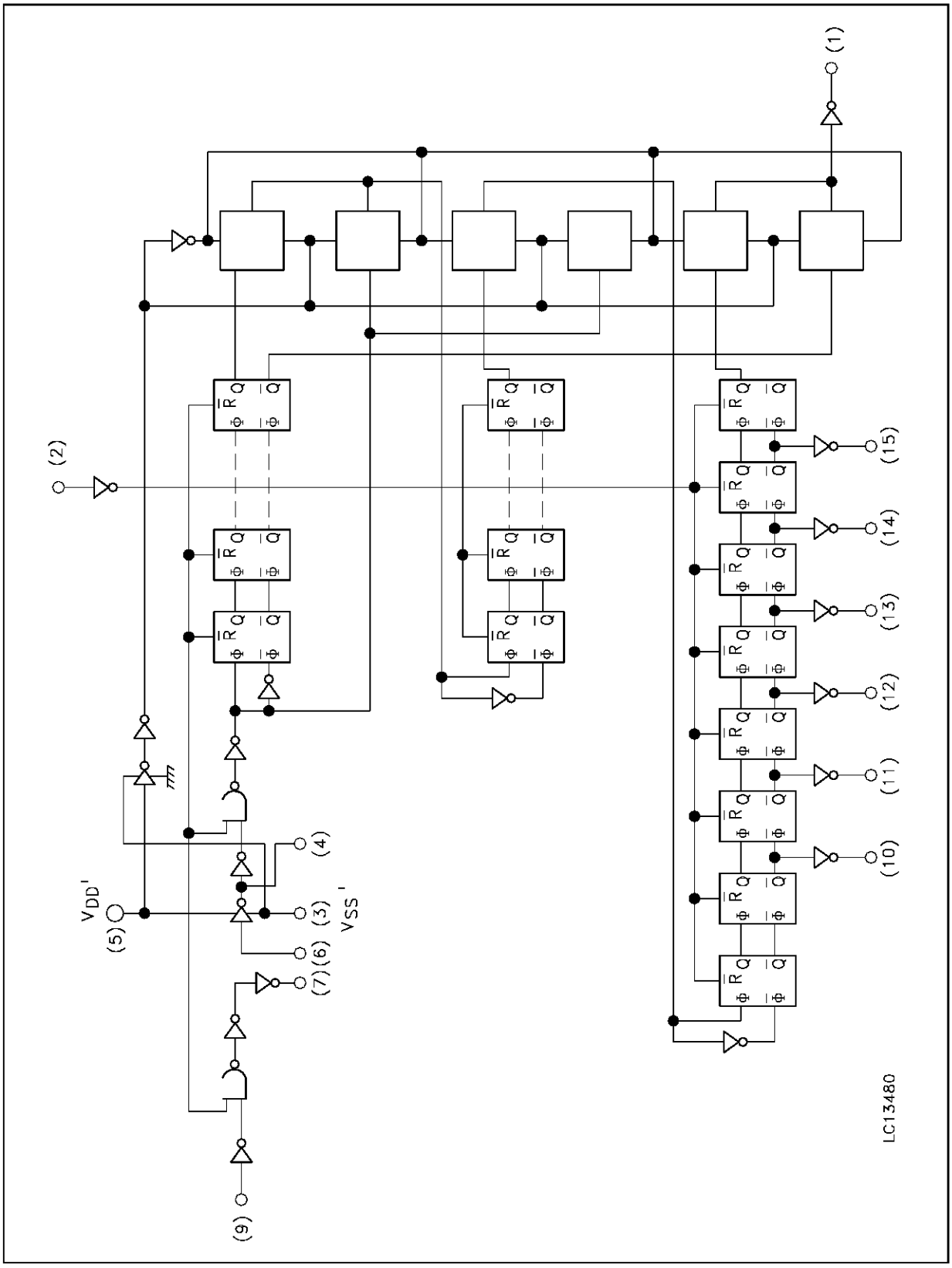
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 15	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-40 to +85	°C

FUNCTIONAL DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions, voltages References to V_{SS})

Symbol	Parameter	Test Conditios				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	-40 °C		25 °C			85 °C		
						Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent Current	0/5			5		20		0.04	20		150	μA
		0/10			10		40		0.04	40		300	
		0/15			15		80		0.04	80		600	
V_{OH}	Output High Voltage	0/5		< 1	5	4.95		4.95			4.95		V
		0/10		< 1	10	9.95		9.95			9.95		
		0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output Low Voltage	5/0		< 1	5		0.05			0.05		0.05	V
		10/0		< 1	10		0.05			0.05		0.05	
		15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input High Voltage		0.5/4.5	< 1	5	3.5		3.5			3.5		V
			1/9	< 1	10	7		7			7		
			1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input Low Voltage		4.5/0.5	< 1	5		1.5			1.5		1.5	V
			9/1	< 1	10		3			3		3	
			13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output Drive Current	0/5	2.5		5	-1.53		-1.36	-3.2		-1.1		mA
		0/5	4.6		5	-0.52		-0.44	-1		-0.36		
		0/10	9.5		10	-1.3		-1.1	-2.6		-0.9		
		0/15	13.5		15	-3.5		-3.0	-6.8		-2.4		
I_{OL}	Output Sink Current	0/5	0.4		5	0.52		0.44	1		0.36		mA
		0/10	0.5		10	1.3		1.1	2.6		0.9		
		0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input Leakage Current	0/18	Any Input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
C_I	Input Capacitance		Any Input						5	7.5			pF

The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5 V, 2 V min. with V_{DD} = 10 V, 2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C, C_L = 50 pF, R_L = 200 KΩ, typical temperature coefficent for all V_{DD} values is 03 %/°C, all input rise and fall times= 20 ns)

Symbol	Parameter	Test Conditions		Value			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}	Output Rise Time		5		100	200	ns
			10		50	100	
			15		40	80	
t_{PHL}	Output Fall Time		5		100	200	ns
			10		50	100	
			15		40	80	
t_{PHL} t_{PLH}	Propagation Delay Time Clock to Q18		5		4.5	9.0	µs
			10		1.7	3.5	
			15		1.3	2.7	
t_{PHL} t_{PLH}	Propagation Delay Time Clock to Q24		5		6.0	12	µs
			10		2.2	4.5	
			15		1.7	3.5	
t_{PHL}	Propagation Delay Time RESET to Qn		5		1300	2600	ns
			10		500	1000	
			15		375	750	
$t_{WH(cl)}$	Clock Pulse Width		5	385	140		ns
			10	150	55		
			15	120	40		
f_{cl}	Clock Pulse Frequency		5		3.5	2	MHz
			10		9	5	
			15		12	6.5	
t_{TLH} t_{THL}	Clock Rise and Fall Time		5			15	µs
			10			15	
			15			15	
$t_{W(R)}$	Reset Pulse Width		5	1400	700		ns
			10	600	300		
			15	450	225		