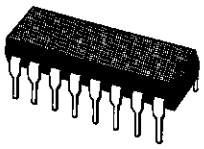
上海双岭电子有限公司

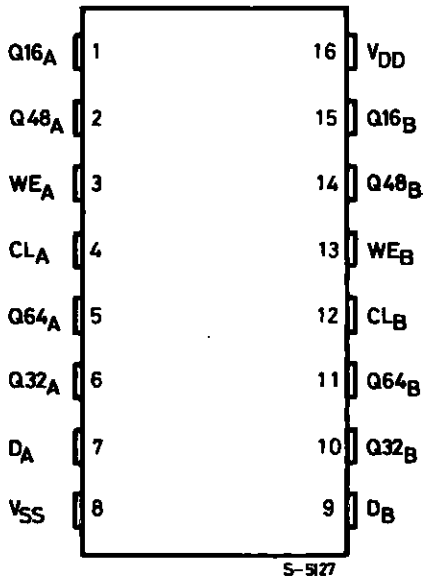
CC4517

DUAL 64-STAGE STATIC SHIFT REGISTER

- CLOCK FREQUENCY 12MHz (TYP.) AT V_{DD} = 10V
- SCHMITT TRIGGER CLOCK INPUTS ALLOW OPERATION WITH VERY SLOW CLOCK RISE AND FALL TIMES
- THREE-STATE OUTPUTS
- QUIESCENT CURRENT SPECIFIED AT 20V FOR HCC DEVICE
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURREN OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



PIN CONNECTIONS

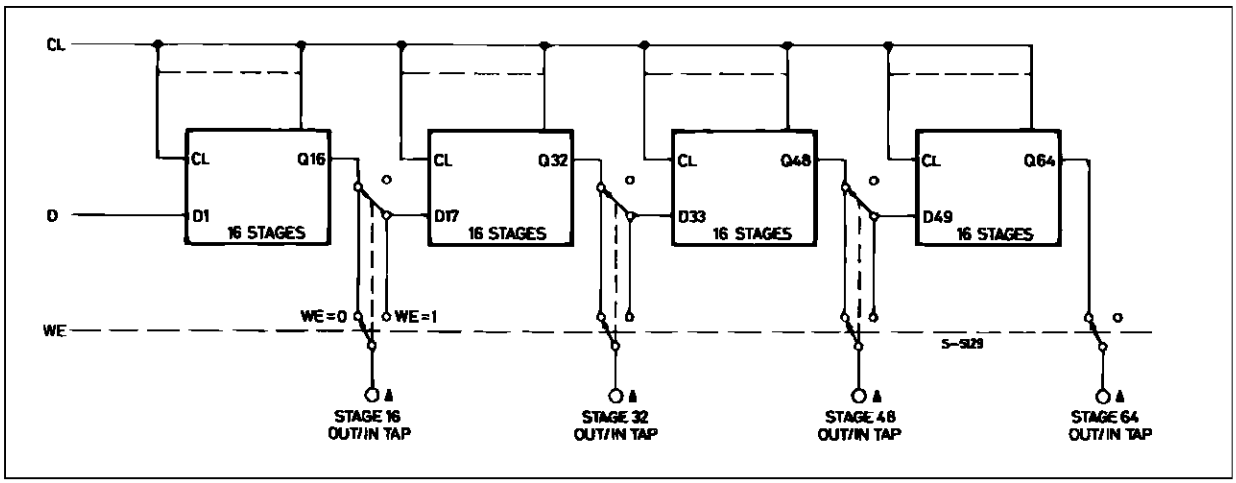


DESCRIPTION

The **CC4517** (extended temperature range) and **CC4517** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package.

The **CC4517** dual 64-stage static shift register consists of two independent registers each having a clock, data, and write enable input and outputs accessible at taps following the 16th, 32nd, 48th, and 64th stages. These taps also serve as input points allowing data to be inputted at the 17th, 33rd, and 49th stages when the write enable input is a logic 1 and the clock goes through a low-to-high transition. The truth table indicates how the clock and write enable inputs control the operation of the **CC4517** . Inputs at the intermediate taps allow entry of 64 bits into the register with 16 clock pulses. The 3-state outputs permit connection of this device to an external bus.

FUNCTIONAL DIAGRAM (one half)



ABSOLUTE MAXIMUM RATINGS

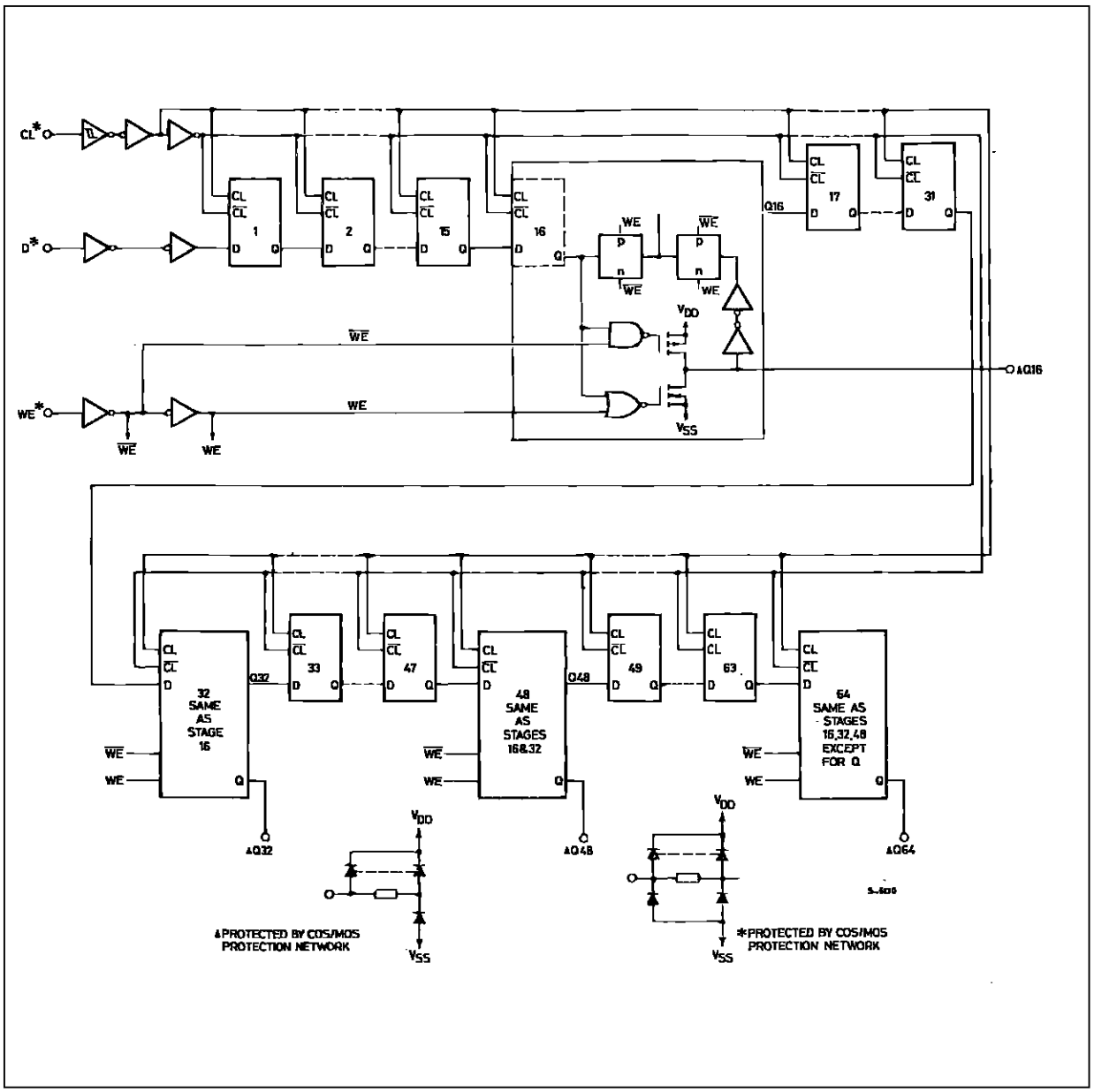
Symbol	Parameter	Value	Unit
V_{DD}*	Supply Voltage :	– 0.5 to + 20	V
V_i	Input Voltage	– 0.5 to V_{DD} + 0.5	V
I_I	DC Input Current (any one input)	± 10	mA
P_{tot}	Total Power Dissipation (per package) Dissipation per Output Transistor for T_{op} = Full Package-temperature Range	200 100	mW mW
T_{op}	Operating Temperature :	– 55 to + 125	°C
T_{stg}	Storage Temperature	– 65 to + 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
* All voltages are with respect to V_{SS} (GND).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage :	3 to 18	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature :	– 55 to + 125	°C

LOGIC DIAGRAM AND TRUTH TABLE



Clock	Write Enable	Data	Stage 16 Tap	Stage 32 Tap	Stage 48 Tap	Stage 64 Tap
0	0	X	Q16	Q32	Q48	Q64
0	1	X	Z	Z	Z	Z
1	0	X	Q16	Q32	Q48	Q64
1	1	X	Z	Z	Z	Z
_/‾	0	DI In	Q16	Q32	Q48	Q64
_/‾	1	Di In	D17 In	D33 In	D49 In	Z
‾_	0	X	Q16	Q32	Q48	Q64
‾_	1	X	Z	Z	Z	Z

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Symbol	Parameter		Test Conditions				Value							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent Current	HCC Types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/18			18		100		0.08	100		3000	
V_{OH}	Output High Voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output Low Voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input High Voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input Low Voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output Drive Current		0/ 5	2.5		5	– 2		– 1.6	– 3.2		– 1.15		mA
			0/ 5	4.6		5	– 0.64		– 0.51	– 1		– 0.36		
			0/10	9.5		10	– 1.6		– 1.3	– 2.6		– 0.9		
			0/15	13.5		15	– 4.2		– 3.4	– 6.8		– 2.4		
I_{OL}	Output Sink Current		0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
I_{IH}, I_{IL}	Input Leakage Current		0/18	Any Input		18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	μA
I_{OH}, I_{OL}	3-State Output Leakage Current		0/18			18		± 0.4		$\pm 10^{-4}$	± 0.4		± 12	μA
C_I	Input Capacitance			Any Input						5	7.5			pF

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, Input t_r, t_f = 20ns, C_L = 50pF, R_L = 200kΩ)

Symbol	Parameter	Test Conditions		Value			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
t_{PHL}, t_{PLH}	Propagation Delay Time : CL to Bit 16 Tap		5		200	400	ns
			10		110	220	
			15		90	180	
t_{PLZ}, t_{PHZ} t_{PZL}, t_{PZH}	3-State Output WE to Bit 16 Tap (see note)		5		75	150	ns
			10		40	80	
			15		30	60	
t_{THL}, t_{TLH}	Output Transition Time		5		100	200	ns
			10		50	100	
			15		40	80	
t_{setup}	Write Enable to Clock		5	– 100	– 50		ns
			10	– 50	– 25		
			15	– 30	– 15		
t_{setup}	Data to Clock		5	– 100	– 50		ns
			10	– 60	– 30		
			15	– 30	– 15		
	Write Enable to Clock Release Time		5		50	100	ns
			10		25	50	
			15		20	40	
t_{hold}	Data to Clock		5		100	200	ns
			10		50	100	
			15		25	50	
t_W	Minimum Clock Pulse Width		5		90	180	ns
			10		40	80	
			15		25	50	
f_{CL}	Maximum Clock Input Frequency		5	3	6		MHz
			10	6	12		
			15	8	15		
t_f, t_r	Maximum Clock Input Rise or Fall Time		5	UNLIMITED			µs
			10				
			15				

Note : Measured at the point of 10% change in output load of 50pF, R_L = 1kΩ to V_{DD} for t_{PZL}, t_{PLZ} and R_L = 1kΩ to V_{SS} for t_{PHZ}.