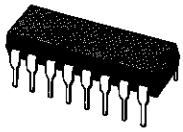
上海双岭电子有限公司

CC4029

PRESETTABLE UP/DOWN COUNTER BINARY OR BCD DECADE

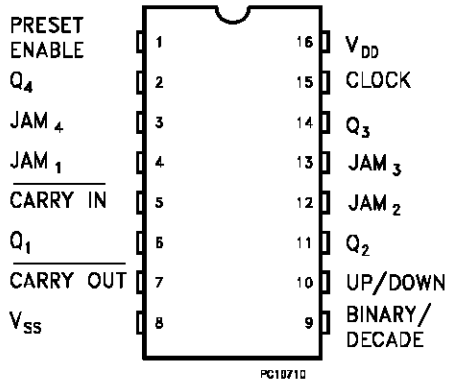
- MEDIUM SPEED OPERATION - 8MHz (typ.) @ C_L = 50pF AND V_{DD}-V_{SS} = 10V
- MULTI-PACKAGE PARALLEL CLOCKING FOR SYNCHRONOUS HIGH SPEED OUTPUT RESPONSE OR RIPPLE CLOCKING FOR SLOW CLOCK INPUT RISE AND FALL TIMES
- "PRESET ENABLE" AND INDIVIDUAL "JAM" INPUTS PROVIDED
- BINARY OR DECADE UP/DOWN COUNTING
- BCD OUTPUTS IN DECADE MODE
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



DESCRIPTION

The **CC4029** (extended temperature range) and **CC4029** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package and plastic micro package. The **CC4029** consists of a four-stage binary or BCD-decade up/down counter with provisions for look-ahead carry in both counting modes. The inputs consist of a single CLOCK, CARRY-IN (CLOCK ENABLE), BINARY/DECADE, UP/DOWN, PRESET ENABLE, and four individual JAM signals. Q1, Q2, Q3, Q4 and a CARRY OUT signal are provided as outputs. A high PRESET ENABLE signal allows information on the JAM INPUTS to preset the counter to any state asynchronously with the clock. A low on each JAM line, when the PRESET-ENABLE signal is high, resets the counter to its zero count. The counter is advanced one count at the positive transition of the clock when the CARRY-IN and PRESET ENABLE signals, are low. Advancement is inhibited when the CARRY-IN or PRESET ENABLE signals are high. The CARRY-OUT signal is normally high and goes low when the

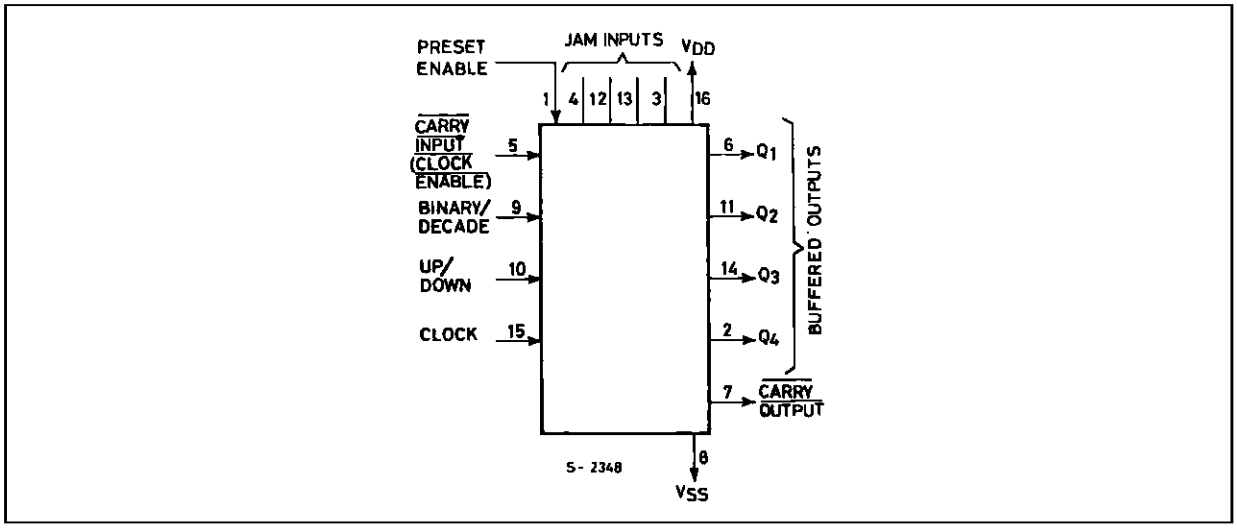
PIN CONNECTIONS



NC = No Internal Connection

counter reaches its maximum count in the UP mode or the minimum count in the DOWN mode provided the CARRY-IN signal is low. The CARRY-IN signal in the low state can thus be considered a CLOCK ENABLE. The CARRY-IN terminal must be connected to V_{SS} when not in use. Binary counting is accomplished when the BINARY/DECADE input is high ; the counter counts in the decade mode when the BINARY/DECADE input is low. The counter counts Up when to UP/DOWN INPUT is high, and Down when the UP/DOWN INPUT is low. Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement as shown in cascading counter packages. Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{DD} *	Supply Voltage:	-0.5 to +20	V V
V_i	Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current (any one input)	± 10	mA
P_{tot}	Total Power Dissipation (per package) Dissipation per Output Transistor for Top = Full Package Temperature Range	200 100	mW mW
T_{op}	Operating Temperature:	-55 to +125	^{o}C o
T_{stg}	Storage Temperature	-65 to +150	^{o}C

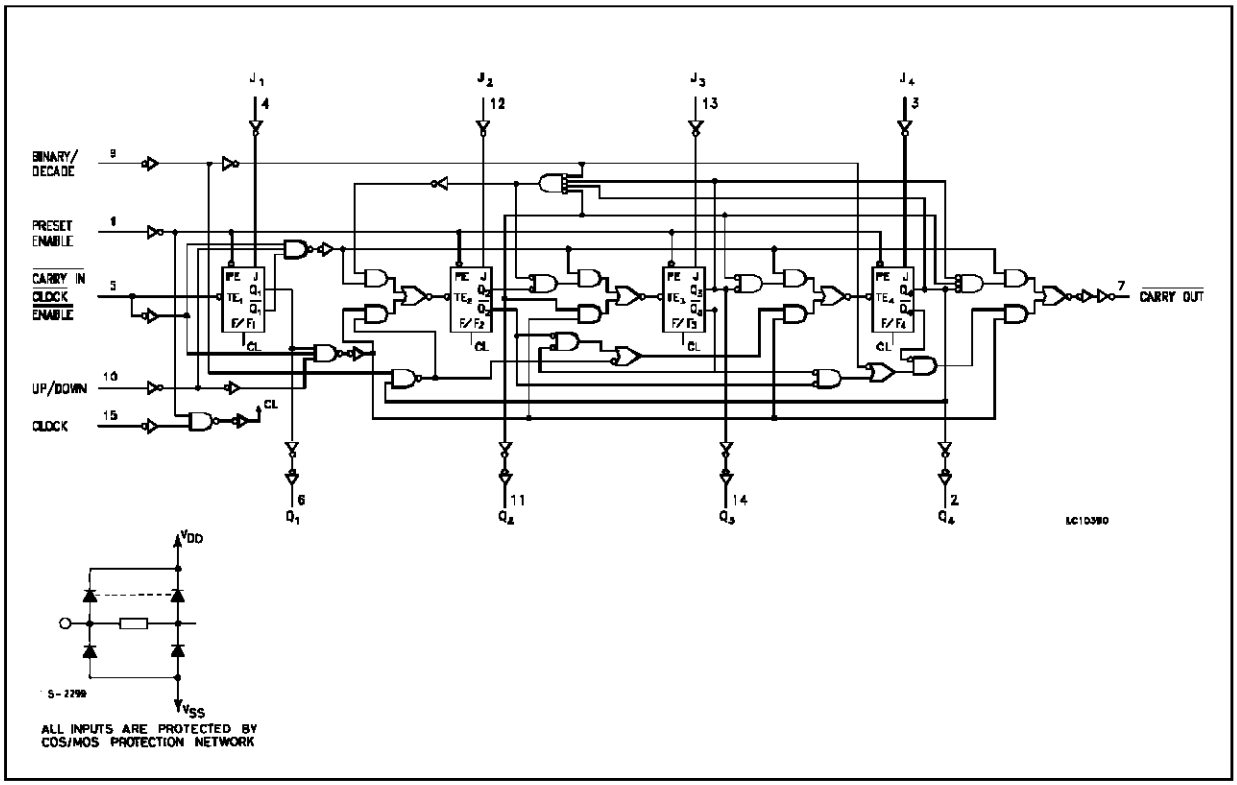
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage:	3 to 18	V V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature:	-55 to +125	^oC ^oC

LOGIC DIAGRAMS



TRUTH TABLES

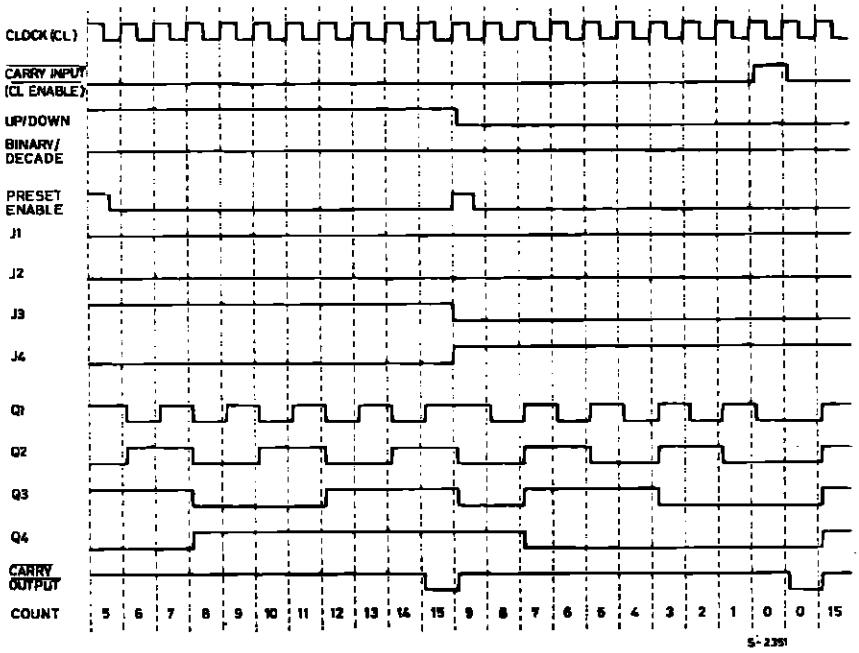
CLOCK	TE	PE	J	Q	$\overline{Q}$
X	X	O	O	O	I
⌝⌞	O	I	X	$\overline{Q}$	Q
X	X	O	I	I	O
⌝⌞	I	I	X	Q	$\overline{Q}$ NC
⌞⌜	X	I	X	Q	$\overline{Q}$ NC

X DON'T CARE

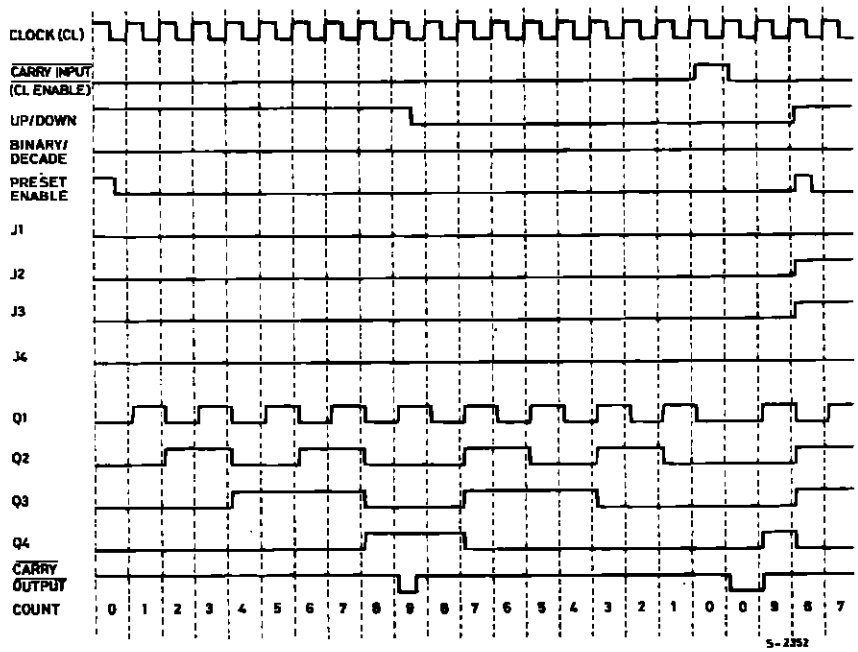
Control Input	Logic Level	Action
BIN/DEC (B/D)	I O	Binary Count Decade Count
UP/DOWN (U/D)	I O	Up Count Down Count
Preset Enable (PE)	I O	Jam In No Jam
Carry In (CI) (Clock Enable)	I O	No Counter Advance at Pos. Clock Transition Advance Counter at Pos. Clock Transition

TIMING DIAGRAMS

Binary Mode



Decade Mode



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Symbol	Parameter	Test Conditios				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (µA)	V_{DD} (V)	T_{LOW} * Min.	T_{LOW} * Max.	25 °C Min.	25 °C Typ.	25 °C Max.	T_{HIGH} * Min.	T_{HIGH} * Max.	
I_L	Quiescent Current	0/5			5		5		0.04	5		150	µA
		0/10			10		10		0.04	10		300	
		0/15			15		20		0.04	20		600	
		0/18			18		100		0.08	100		3000	
V_{OH}	Output High Voltage	0/5		< 1	5	4.95		4.95			4.95		V
		0/10		< 1	10	9.95		9.95			9.95		
		0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output Low Voltage	5/0		< 1	5		0.05			0.05		0.05	V
		10/0		< 1	10		0.05			0.05		0.05	
		15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input High Voltage		0.5/4.5	< 1	5	3.5		3.5			3.5		V
			1/9	< 1	10	7		7			7		
			1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input Low Voltage		4.5/0.5	< 1	5		1.5			1.5		1.5	V
			9/1	< 1	10		3			3		3	
			13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output Drive Current	0/5	2.5		5	-2		-1.6	-3.2		-1.15		mA
		0/5	4.6		5	-0.64		-0.51	-1		-0.36		
		0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
		0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
I_{OL}	Output Sink Current	0/5	0.4		5	0.64		0.51	1		0.36		mA
		0/10	0.5		10	1.6		1.3	2.6		0.9		
		0/15	1.5		15	4.2		3.4	6.8		2.4		
I_{IH}, I_{IL}	Input Leakage Current	0/18	Any Input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	µA
C_I	Input Capacitance		Any Input						5	7.5			pF