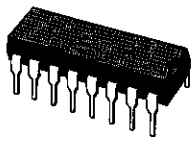
DUAL-J-K MASTER-SLAVE FLIP-FLOP

- SET-RESET CAPABILITY
- STATIC FLIP-FLOP OPERATION - RETAINS STATE INDEFINITELY WITH CLOCK LEVEL EITHER "HIGH" OR "LOW"
- MEDIUM SPEED OPERATION - 16MHz (typ. clock toggle rate at 10V)
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES".



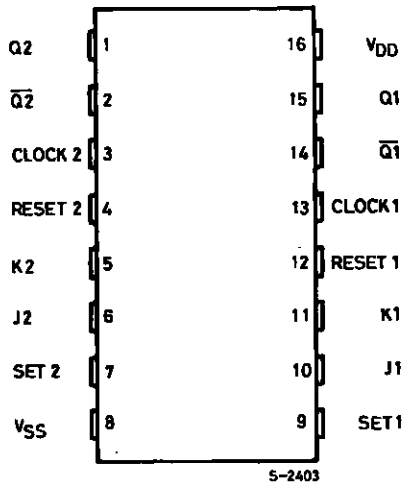
DESCRIPTION

The **CC4027** (extended temperature range) and **CC4027** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package and plastic micro package.

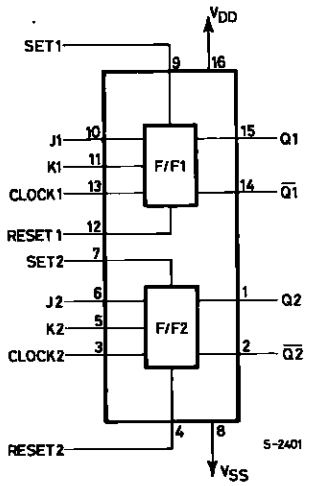
The **CC4027** is a single monolithic chip integrated circuit containing two identical complementary-symmetry J-K master-slave flip-flops. Each flip-flop has provisions for individual J, K, Set, Reset, and Clock input signals, Buffered Q and $\overline{Q}$ signals are provided as outputs. This input-output arrangement provides for compatible operation with the **CC4027** dual D-type flip-flop.

The **CC4027** is useful in performing control, register, and toggle functions. Logic levels present at the J and K inputs along with internal self-steering control the state of each flip-flop ; changes in the flip-flop state are synchronous with the positive-going transition of the clock pulse. Set and reset functions are independent of the clock and are initiated when a high level signal is present at either the Set or Reset input.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}*	Supply Voltage :	– 0.5 to + 18	V
V_i	Input Voltage	– 0.5 to V_{DD} + 0.5	V
I_I	DC Input Current (any one input)	± 10	mA
P_{tot}	Total Power Dissipation (per package) Dissipation per Output Transistor for T_{op} = Full Package-temperature Range	200 100	mW mW
T_{op}	Operating Temperature :	– 55 to + 125	°C °
T_{stg}	Storage Temperature	– 65 to + 150	°C

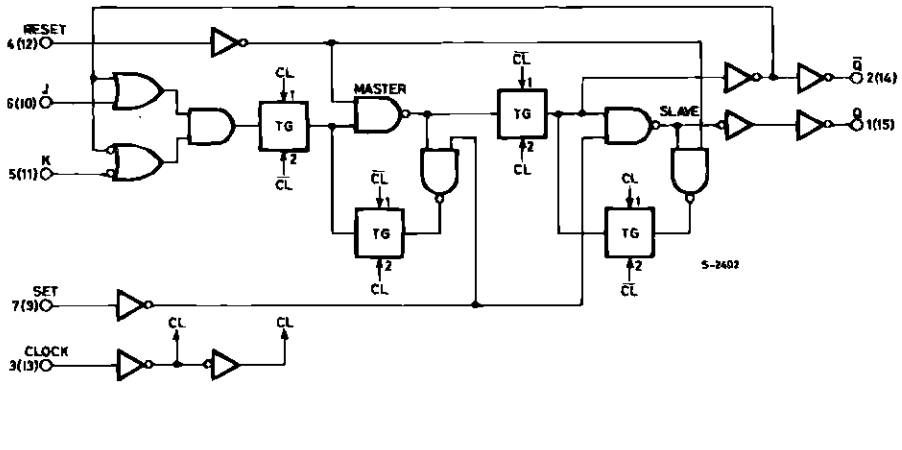
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.
* All voltage values are referred to V_{SS} pin voltage .

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage :	3 to 18	V V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature : **HCC** Types	– 55 to + 125	°C °

LOGIC DIAGRAM AND TRUTH TABLE

ONE OF TWO IDENTICAL J-K FLIP-FLOPS



TRUTH TABLE

Present State					CL$^{\Delta}$	Next State		
Inputs				Output		Outputs		
J	K	S	R	Q		Q	$\overline{Q}$	
I	X	O	O	O	_/‾	I	O	
X	O	O	O	I	_/‾	I	O	
O	X	O	O	O	_/‾	O	I	
X	I	O	O	I	_/‾	O	I	
X	X	O	O	X	‾_			← No Change
X	X	I	O	X	X	I	O	
X	X	O	I	X	X	O	I	
X	X	I	I	X	X	I	I	

LOGIC I = HIGH LEVEL
LOGIC O = LOW LEVEL
Δ - LEVEL CHANGE
X - DON'T CARE

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Symbol	Parameter	Test Conditions				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
						Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent Current	0/ 5			5		1		0.02	1		30	μA
		0/10			10		2		0.02	2		60	
		0/15			15		4		0.02	4		120	
		0/18			18		20		0.04	20		600	
V_{OH}	Output High Voltage	0/ 5		< 1	5	4.95		4.95			4.95		V
		0/10		< 1	10	9.95		9.95			9.95		
		0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output Low Voltage	5/0		< 1	5		0.05			0.05		0.05	V
		10/0		< 1	10		0.05			0.05		0.05	
		15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input High Voltage		0.5/4.5	< 1	5	3.5		3.5			3.5		V
			1/9	< 1	10	7		7			7		
			1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input Low Voltage		4.5/0.5	< 1	5		1.5			1.5		1.5	V
			9/1	< 1	10		3			3		3	
			13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output Drive Current	0/ 5	2.5		5	– 2		– 1.6	– 3.2		– 1.15		mA
		0/ 5	4.6		5	– 0.64		– 0.51	– 1		– 0.36		
		0/10	9.5		10	– 1.6		– 1.3	– 2.6		– 0.9		
		0/15	13.5		15	– 4.2		– 3.4	– 6.8		– 2.4		
I_{OL}	Output Sink Current	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
		0/10	0.5		10	1.6		1.3	2.6		0.9		
		0/15	1.5		15	4.2		3.4	6.8		2.4		
I_{IH}, I_{IL}	Input Leakage Current	0/18	Any Input		18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	μA
C_I	Input Capacitance		Any Input						5	7.5			pF

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200kΩ, typical temperature coefficient for all V_{DD} = 0.3%/°C values, all input rise and fall time = 20ns)

Symbol	Parameter		Test Conditions	Value			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay Time	Clock to Q or $\overline{Q}$ Outputs	5		150	300	ns
			10		65	130	
			15		45	90	
t_{PLH}	Propagation Delay Time	Set to Q or Reset to $\overline{Q}$	5		150	300	ns
			10		65	130	
			15		45	90	
t_{PHL}	Propagation Delay Time	Set to $\overline{Q}$ or Reset to Q	5		200	400	
			10		85	170	
			15		60	120	
t_{THL}, t_{TLH}	Transition Time		5		100	200	ns
			10		50	100	
			15		40	80	
t_W	Pulse Width	Clock	5	140	70		ns
			10	60	30		
			15	40	20		
t_W	Pulse Width	Set or Reset	5	180	90		
			10	80	40		
			15	50	25		
t_r,t_f	Clock Input Rise or Fall Time		5			15	µs
			10			4	
			15			1	
t_{setup}	Setup Time	Data	5	200	100		ns
			10	75	35		
			15	50	25		
f_{max}	Maximum Clock Input Frequency *	Toggle Mode	5	3.5	7		MHz
			10	8	16		
			15	12	24		

* Input tr, tf = 5ns.